



Atty. Dkt. No. 035905-0104

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Thomas H. LEE et al.

Title: DENSE ARRAYS AND CHARGE STORAGE DEVICES AND METHODS FOR MAKING SAME

Appl. No.: 09/927,648

Filing Date: August 13, 2001

Examiner: Unassigned

Art Unit: 2818



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INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO-1449 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), before the mailing of the first official action.

RELEVANCE OF EACH DOCUMENT

All of the documents are in English.

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO-1449 be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Respectfully submitted,

Date: _____

11/27/01

FOLEY & LARDNER
3000 K Street, NW, Suite 500
Washington, DC 20007
Telephone: (202) 672-5300
Facsimile: (202) 672-5399

By _____



Leon Radomsky
Registration No. 43,445

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Substitute for form 1449B/PTO		C mplete if Kn wn	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicati n Number	09/927,648
Date Submitted: November 27, 2001		Filing Dat	08/13/2001
(use as many sheets as necessary)		First Named Inventor	Thomas H. Lee et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
Sheet	1	Attorney Docket Number	035905/0104

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	A51	5,427,979		Chang	6/27/1995	
	A52	5,070,384		McCollum et al.	12/3/1991	
	A53	4,498,226		Inoue et al.	2/12/1985	
	A54	4,489,478		Sakurai	12/25/1984	
	A55	4,272,880		Pashley	6/16/1981	
	A56	5,745,407		Levy et al.	4/28/1998	
	A57	5,535,156		Levy et al.	7/9/1996	
	A58	4,499,557		Holmberg et al.	2/12/1985	
	A59	4,442,507		Roesner	4/10/1984	
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	A61	4,543,594		Mohsen et al.	9/24/1985	
	A62	4,569,121		Lim et al.	2/11/1986	
	A63	4,646,266		Ovshinsky et al.	2/24/1987	
	A64	4,820,657		Hughes et al.	4/11/1989	
	A65	4,823,181		Mohsen et al.	4/18/1989	
	A66	4,811,114		Yamamoto et al.	3/7/1989	
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	A68	3,863,231		Taylor	1/28/1975	
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	A70	4,146,902		Tanimoto et al.	3/27/1979	
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	A73	4,281,397		Neal et al.	7/28/1981	
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	A77	4,922,319		Fukushima	5/1/1990	
	A78	4,943,538		Mohsen et al.	7/24/1990	
	A79	5,070,383		Sinar et al.	5,070,383	
	A80	5,311,039		Kimura et al.	5,311,039	
	A81	5,334,880		Abadeer et al.	5,334,880	
	A82	5,391,907		Jang	2/21/1995	
	A83	5,441,907		Sung et al.	5,441,907	
	A84	5,463,244		De Araujo et al.	5,463,244	
	A85	5,536,968		Crafts et al.	7/16/1996	
	A86	5,675,547		Koga	10/7/1997	
	A87	5,737,259		Chang	4/7/1998	
	A88	5,751,012		Wolstenholme et al.	5/12/1998	
	A89	5,776,810		Guterman et al.	7/7/1998	
	A90	5,835,396		Zhang	11/10/1998	

Examiner Signature	Date Considered
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				Group Art Unit	2818
				Examiner Name	Unassigned
				Attorney Docket Number	035905/0104
Sheet	2	of	7		

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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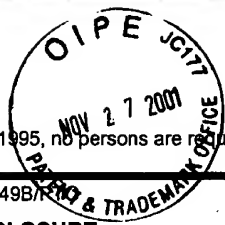
OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ⁶
	A115 ✓ a	JOHN H. DOUGLAS: "The Route to 3-D Chips," High Technology, September 1983, pgs. 55-59, Vol. 3, No. 9, High Technology Publishing Corporation, Boston, MA			
	A116 ✓ b	M. ARIENZO et al.: "Diffusion of Arsenic in Bilayer Polycrystalline Silicon Films," J. Appl. Phys., January 1984, pgs. 365-369, Vol. 55, No. 2, American Institute of Physics			
	A117 ✓ c	O. BELLEZZA et al.: "A New Self-Aligned Field Oxide Cell for Multimegabit Eproms," IEDM, pgs. 579-582, IEEE			
	A118 ✓ d	S.D. BROTHERTON et al.: "Excimer-Laser-Annealed Poly-Si Thin-Film Transistors," IEEE Transactions on Electron Devices, February 1993, pgs. 407-413, Vol. 40, No. 2, IEEE			
	A119 ✓ e	P. CANDELIER et al.: "Simplified 0.35-μm Flash EEPROM Process Using High-Temperature Oxide (HTO) Deposited by LPCVD as Interpoly Dielectrics and Peripheral Transistors Gate Oxide," IEEE Electron Device Letters, July 1997, pgs. 306-308, Vol. 18, No. 7, IEEE			
	A120 ✓ f	MIN CAO et al.: "A High-Performance Polysilicon Thin-Film Transistor Using XeCl Excimer Laser Crystallization of Pre-Patterned Amorphous Si Films," IEEE Transactions on Electron Devices, April 1996, pgs. 561-567, Vol. 43, No. 4, IEEE			
	A121 ✓ g	MINO CAO et al.: "A Simple EEPROM Cell Using Twin Polysilicon Thin Film Transistors," IEEE Electron Device Letters, August 1994, pgs. 304-306, Vol. 15, No. 8, IEEE			
	A122 ✓ h	BOMY CHEN et al.: "Yield Improvement for a 3.5-ns BICMOS Technology in a 200-mm Manufacturing Line," IBM Technology Products, 1993, pgs.301-305, VLSITSA			
	A123 ✓ i	VICTOR W.C. CHAN et al.: "Three Dimensional CMOS Integrated Circuits on Large Grain Polysilicon Films," IEDM, 2000, IEEE			
	A124 ✓ j	BOAZ EITAN et al.: "Alternate Metal Virtual Ground (AMG) - A New Scaling Concept for Very High-Density EPROM's," IEEE Electron Device Letters, pgs. 450-452, Vol. 12, No. 8, August 1991, IEEE			

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Substitute for form 1449B/ INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: <u>November 27, 2001</u> (use as many sheets as necessary)		Complete If Known	
		Application Number	09/927,648
		Filing Date	08/13/2001
		First Named Inventor	Thomas H. Lee et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
		Attorney Docket Number	035905/0104
Sheet	4	of	7

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A125 ✓	BOAZ EITAN et al.: "Multilevel Flash cells and their Trade-offs," IEEE Electron Device Letters, pgs. 169-172, 1996, IEEE	
	A126 ✓	DR. HEINRICH ENDERT: "Excimer Lasers as Tools for Material Processing in Manufacturing," Technical Digest: International Electron Devices Meeting, 1985, pgs. 28-29, Washington, DC, December 1-4, 1985, Göttingen, Germany	
	A127 ✓	DOV FROHMAN-BENTCHKOWSKY: "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, pgs. 301-306, Vol. sc-6, No. 5, October 1971	
	A128 ✓	G.K. GIUST et al.: "Laser-Processed Thin-Film Transistors Fabricated from Sputtered Amorphous-Silicon Films," IEEE Transactions on Electron Devices, pgs. 207-213, Vol. 47, No. 1, January 2000, IEEE	
	A129 ✓	G.K. GIUST et al.: "High-Performance Thin-Film Transistors Fabricated Using Excimer Laser Processing and Grain Engineering," IEEE Transactions on Electron Devices, pgs. 925-932, Vol. 45, No. 4, April 1998, IEEE	
	A130 ✓	G.K. GIUST et al.: "High-Performance Laser-Processed Polysilicon Thin-Film Transistors," IEE Electron Device Letters, pgs. 77-79, Vol. 20, No. 2, February 1999, IEEE	
	A131 ✓	FUMIHIKO HAYASHI et al.: "A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pgs. 87-88, Stanford University, Stanford, CA 94305, USA	
	A132 ✓	STEPHEN C.H. HO et al.: "Thermal Stability of Nickel Silicides in Different Silicon Substrates," Department of Electrical and Electronic Engineering, pgs. 105-108, 1998, IEEE	
	A133 ✓	J. ESQUIVEL et al.: "High Density Contactless, Self Aligned EPROM Cell Array Technology," Texas Instruments (Dallas), IEDM 86, pgs. 592-595, 1986, IEEE	

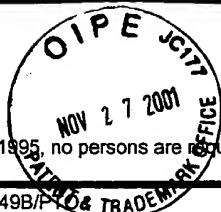
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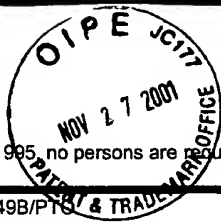
OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ^a
	A134 ✓	R. KAZEROUNIAN et al.: Alternate Metal Virtual Ground EPROM Array Implemented in a 0.8µm Process for Very High Density Applications," IEDM 91, pgs. 311-314, 1991, IEEE	
	A135 ✓	CHANG-DONG KIM et al.: "Short-Channel Amorphous-Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, pgs. 2172-2176, Vol. 43, No. 12, December 1996, IEEE	
	A136 ✓	JOHAN H. KLOOTWIJK et al.: "Deposited Inter-Polysilicon Dielectrics for Nonvolatile Memories," IEEE Transactions on Electron Devices, pgs. 1435-1445, Vol. 46, No. 7, July 1999, IEEE	
	A137 ✓	WEBPAGE - JA-HUM KU et al.: "High Performance pMOSFETs With Ni(Si/sub x/Ge/sub 1-x Si/Sub 0.8/Ge/sub 0.2/ gate, IEEE Xplore Citation," VLSI Technology, 200. Digest of Technical Paper Symposium on page(s): 114-115 June 13-15 2000	
	A138 ✓	NAE-IN LEE et al.: "High-Performance EEPROM's Using N- and P-Channel Polysilicon Thin-Film Transistors with Electron Cyclotron Resonance N2O-Plasma Oxide," pgs. 15-17, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IEEE	
	A139 ✓	JIN-WOO LEE et al.: "Improved Stability of Polysilicon Thin-Film Transistors under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel," IEEE Electron Device Letters, 1998, pgs. 265-268, IEEE	
	A140 ✓	SEOK-WOON LEE et al.: "Pd induced lateral crystallization of Amorphous Si Thin Films," Appl. Phys. Lett. 66 (13), pgs. 1671-1673, 27 March 1995, American Institute of Physics	
	A141 ✓	K. MIYASHITA et al.: "Optimized Halo Structure for 80 nm Physical Gate CMOS Technology with Indium and Antimony Highly Angled Ion Implantation," IEDM 99-645, pgs. 27.2.1-27.2.4, 1999, IEEE	
	A142 ✓	N.D. YOUNG et al.: "The Fabrication and Characterization of EEPROM Arrays on Glass Using a Low-Temperature Poly-Si TFT Process," IEEE Transactions on Electron Devices, pgs. 1930-1936, Vol. 43, No. 11, November 1996, IEEE	

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	A143 ✓	JUNG-HOON OH et al.: "A High-Endurance Low-Temperature Polysilicon Thin-Film Transistor EEPROM Cell," pgs. 304-306, IEEE Electron Device Letters, Vol. 21, No. 6, June 2000, IEEE		
	A144 ✓	WEBPAGE - M.C. POON. et al.: "Thermal Stability of Cobalt and Nickel Silicides in Amorphous Crystalline Silicon," pg. 1, IEEE Xplore, Electron Devices Meeting, 1997, Proceedings, 19 Hong Kong, 2000, IEEE		
	A145 ✓	NORIAKI SATO et al.: "A New Programmable Cell Utilizing Insulator Breakdown," IEDM 85, pgs. 639-642, 1985, IEEE		
	A146 ✓	TAKEO SHIBA et al.: "In Situ Phosphorus-Doped Polysilicon Emitter Technology for Very High-Speed, Small Emitter Bipolar Transistors," IEEE Transactions on Electron Devices, pgs. 889-897, Vol. 43, No. 6, June 1996, IEEE		
	A147 ✓	SEUNGHEON SONG et al.: "High Performance Transistors with State-of-the-Art CMOS Technologies," IEDM 99, pgs. 427-430, 1999, IEEE		
	A148 ✓	YOSHIHIRO TAKAO et al.: "Low-Power and High-Stability SRAM Technology Using a Laser-Recrystallized p-Channel SOI MOSFET," IEEE Transactions on Electron Devices, pgs. 2147-2152, Vol. 39, No. 9, September 1992, IEEE		
	A149 ✓	KENJI TANIGUCHI et al.: "Process Modeling and Simulation: Boundary Conditions for Point Defect-Based Impurity Diffusion Model," IEEE Transactions on Computer-Aided Design, pgs. 1177-1183, Vol. 9, No. 11, November 1990, IEEE		
	A150 ✓	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, pgs. 391-393, Vol. 21, No. 9, September 2000, IEEE		
	A151 ✓	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, Vol. 21, No. 9, pgs. 439-441, September 2000, IEEE		

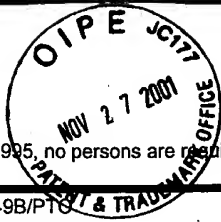
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		First Named Inventor	Thomas H. Lee et al.
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		Examiner Name	Unassigned
		Attorney Docket Number	035905/0104
Sheet	7	of	7

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
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